

## 128K x 16 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

OCTOBER 2005

### FEATURES

- High-speed access time: 8, 10 ns
- Operating Current: 50mA (typ.)
- Stand by Current: 700µA (typ.)
- TTL and CMOS compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

### DESCRIPTION

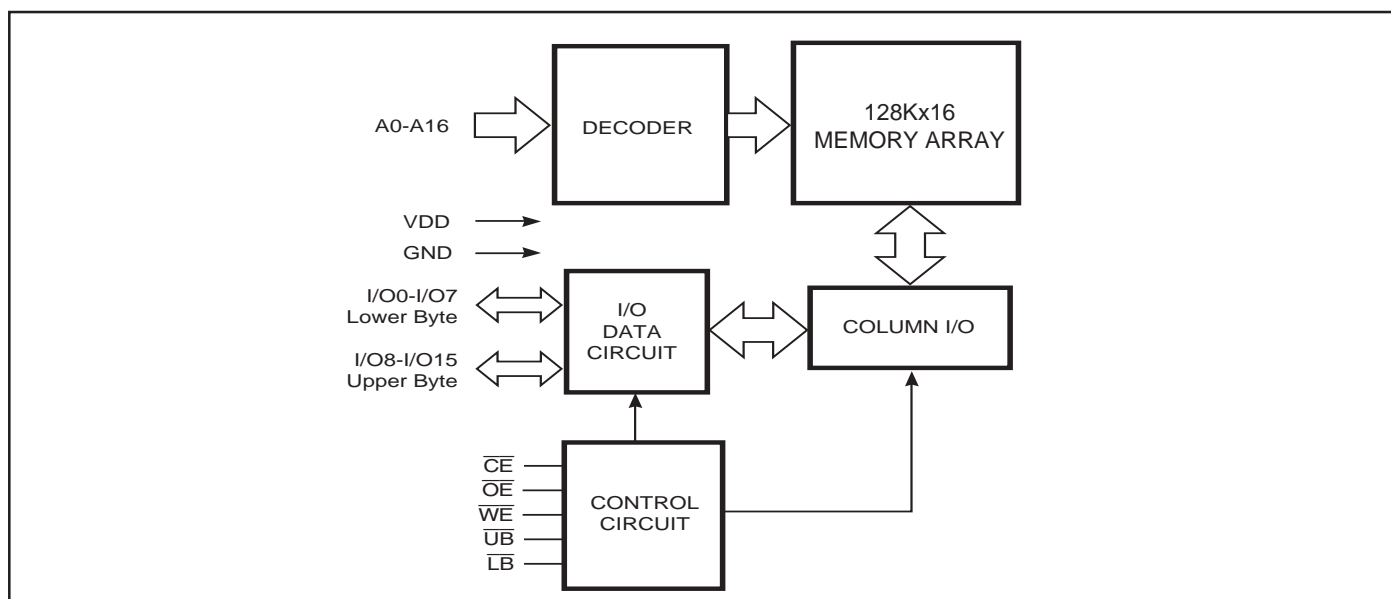
The *ISSI* IS61LV12816L is a high-speed, 2,097,152-bit static RAM organized as 131,072 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs,  $\overline{CE}$  and  $\overline{OE}$ . The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS61LV12816L is packaged in the JEDEC standard 44-pin TSOP (Type II), 44-pin LQFP, and 48-pin mini BGA (6mm x 8mm).

### FUNCTIONAL BLOCK DIAGRAM

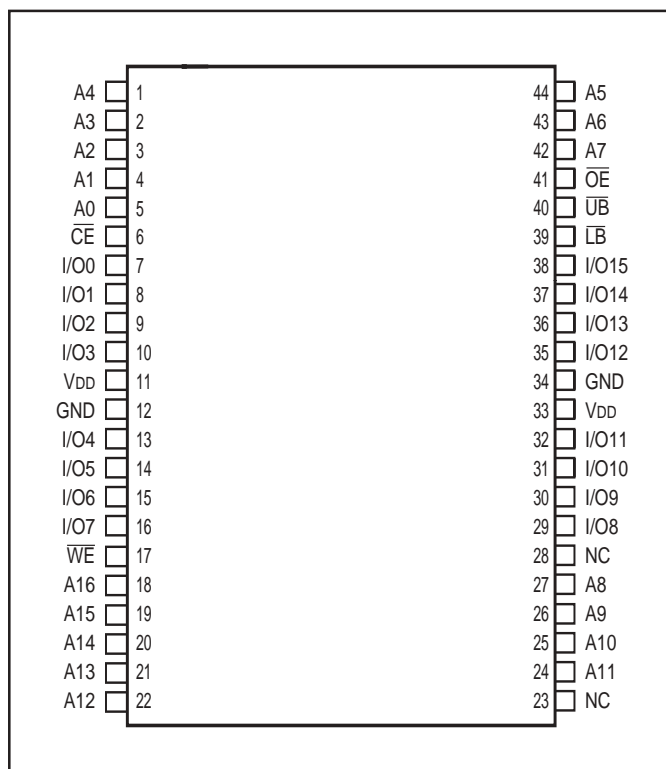


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**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V <sub>DD</sub> Current
						I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	X	X	High-Z	High-Z	I <sub>CC</sub>
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D <sub>OUT</sub>	High-Z	I <sub>CC</sub>
	H	L	L	H	L	High-Z	D <sub>OUT</sub>	
	H	L	L	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	L	X	L	H	D <sub>IN</sub>	High-Z	I <sub>CC</sub>
	L	L	X	H	L	High-Z	D <sub>IN</sub>	
	L	L	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

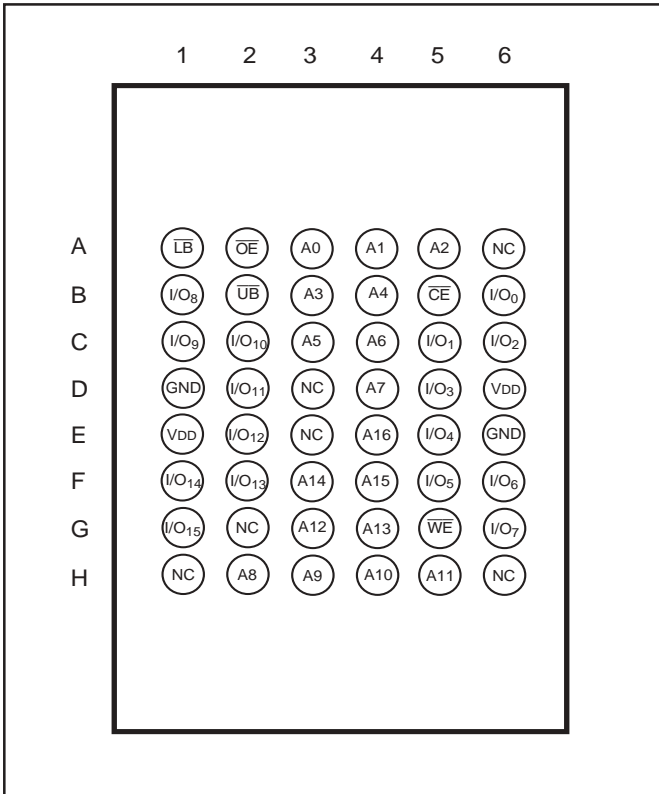
**PIN CONFIGURATION**  
44-Pin TSOP (Type II) (T)



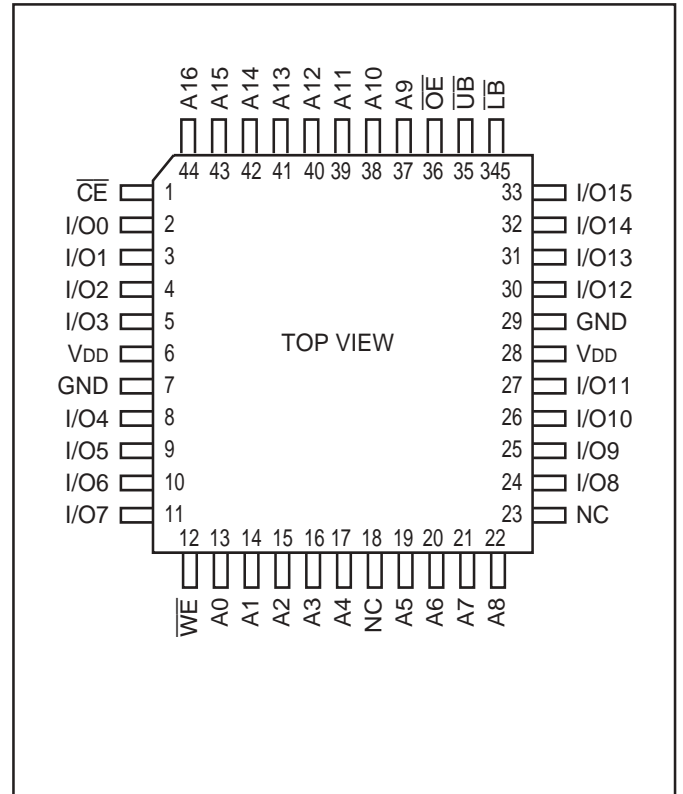
**PIN DESCRIPTIONS**

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V <sub>DD</sub>	Power
GND	Ground

**PIN CONFIGURATION**  
48-Pin mini BGA (B)



44-Pin LQFP (LQ)



**PIN DESCRIPTIONS**

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Power Supply Voltage Relative to GND	-0.5 to 4.0V	V
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> + 0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to + 150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE**

Range	Ambient Temperature	V <sub>DD</sub> (8 ns)	V <sub>DD</sub> (10 ns)
Commercial	0°C to +70°C	3.3V + 10%, -5%	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V + 10%, -5%	3.3V ± 10%

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>(1)</sup>		2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled	-1	1	μA

**Note:**

1. V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width - 2.0 ns). Not 100% tested.  
V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width - 2.0 ns). Not 100% tested.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns		-10 ns		Unit
				Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CE}$ = V <sub>IL</sub> I <sub>OUT</sub> = 0 mA, f = Max.	Com.	—	65	—	60	mA
			Ind.	—	70	—	65	
			typ. <sup>(2)</sup>	—	50	—	50	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE} \geq V_{IH}$ , f = max	Com.	—	30	—	25	mA
			Ind.	—	35	—	30	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CE} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> $\geq$ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> $\leq$ 0.2V, f = 0	Com.	—	3	—	3	mA
			Ind.	—	4	—	4	mA
			typ. <sup>(2)</sup>	—	700	—	700	$\mu$ A

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub>=3.3V, T<sub>A</sub>=25°C. Not 100% tested.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Note:**

- Tested initially and after any design or process changes that may affect these parameters.

## AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

## AC TEST LOADS

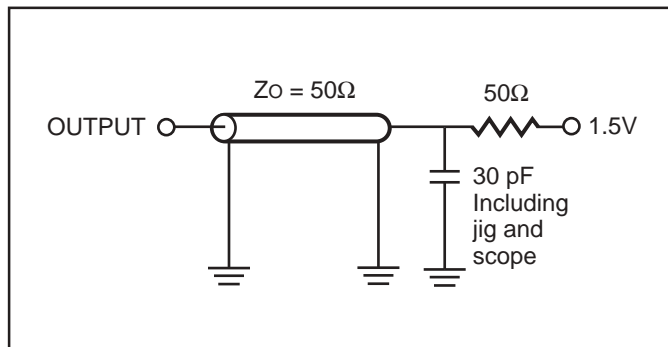


Figure 1.

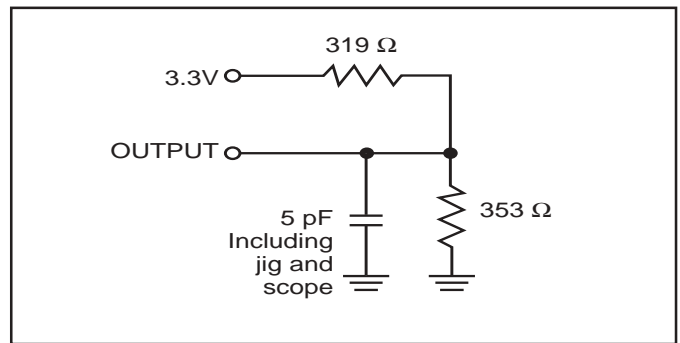


Figure 2.

READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

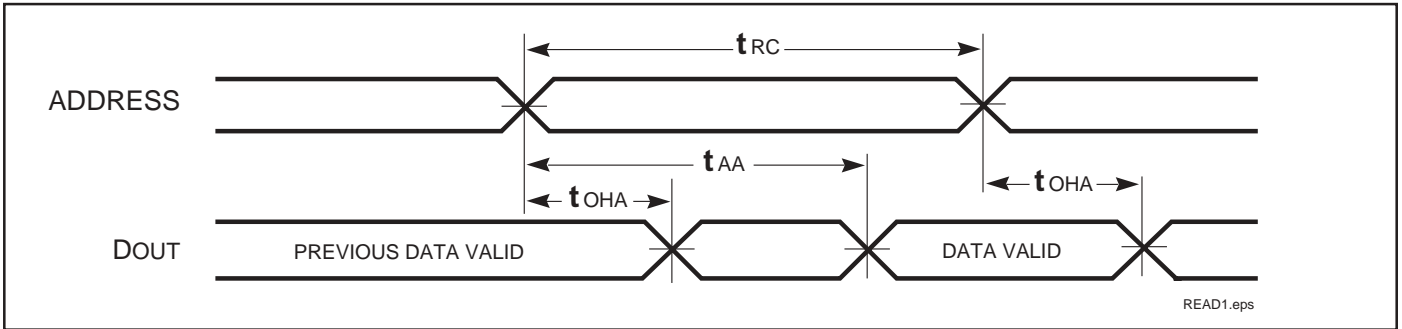
Symbol	Parameter	-8 ns		-10 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	8	—	10	—	ns
t <sub>AA</sub>	Address Access Time	—	8	—	10	ns
t <sub>OHA</sub>	Output Hold Time	3	—	3	—	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ Access Time	—	8	—	10	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ Access Time	—	3.5	—	4	ns
t <sub>HZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to High-Z Output	—	3.5	—	4	ns
t <sub>LZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	ns
t <sub>HZCE</sub> <sup>(2)</sup>	$\overline{\text{CE}}$ to High-Z Output	0	3.5	0	4	ns
t <sub>LZCE</sub> <sup>(2)</sup>	$\overline{\text{CE}}$ to Low-Z Output	3.5	—	3	—	ns
t <sub>BA</sub>	$\overline{\text{LB}}, \overline{\text{UB}}$ Access Time	—	3.5	—	4	ns
t <sub>HZB</sub> <sup>(2)</sup>	$\overline{\text{LB}}, \overline{\text{UB}}$ to High-Z Output	0	3.5	0	4	ns
t <sub>LZB</sub> <sup>(2)</sup>	$\overline{\text{LB}}, \overline{\text{UB}}$ to Low-Z Output	0	—	0	—	ns

## Notes:

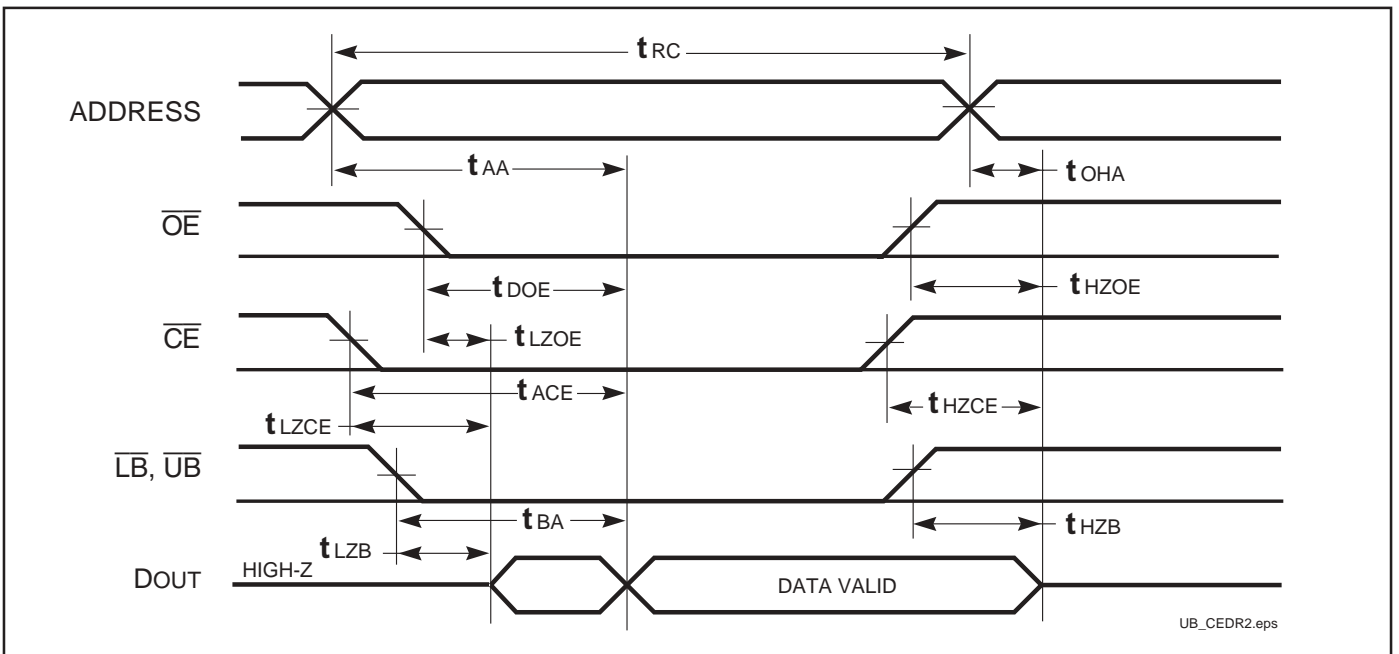
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) ( $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ )



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup> (Over Operating Range)

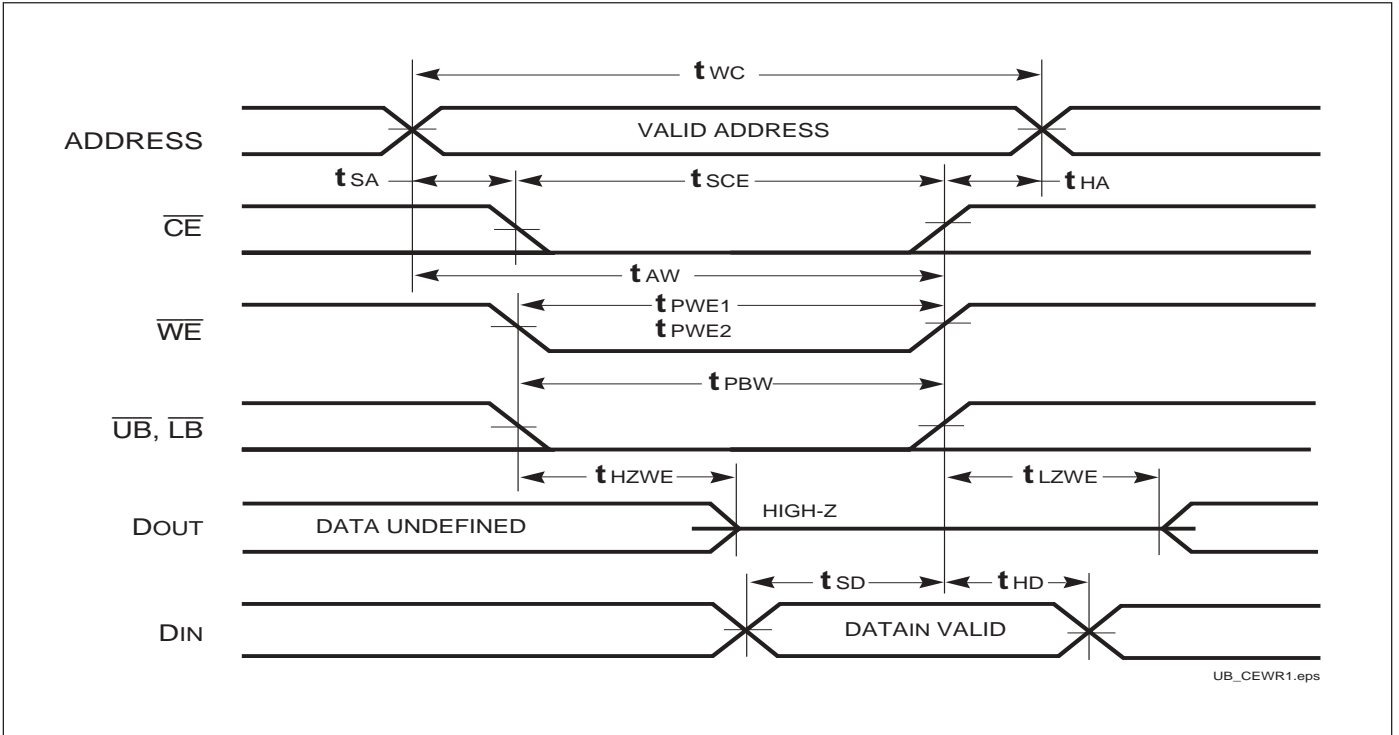
Symbol	Parameter	-8 ns		-10 ns		Unit
		Min.	Max	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	8	—	10	—	ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	7	—	8	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	7	—	8	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PBW</sub>	$\overline{LB}$ , $\overline{UB}$ Valid to End of Write	6.5	—	8	—	ns
t <sub>PWE1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = HIGH)	6	—	7	—	ns
t <sub>PWE2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = LOW)	6.5	—	8	—	ns
t <sub>SD</sub>	Data Setup to Write End	4	—	5	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	$\overline{WE}$ LOW to High-Z Output	—	3	—	4	ns
t <sub>LZWE</sub> <sup>(3)</sup>	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

**Notes:**

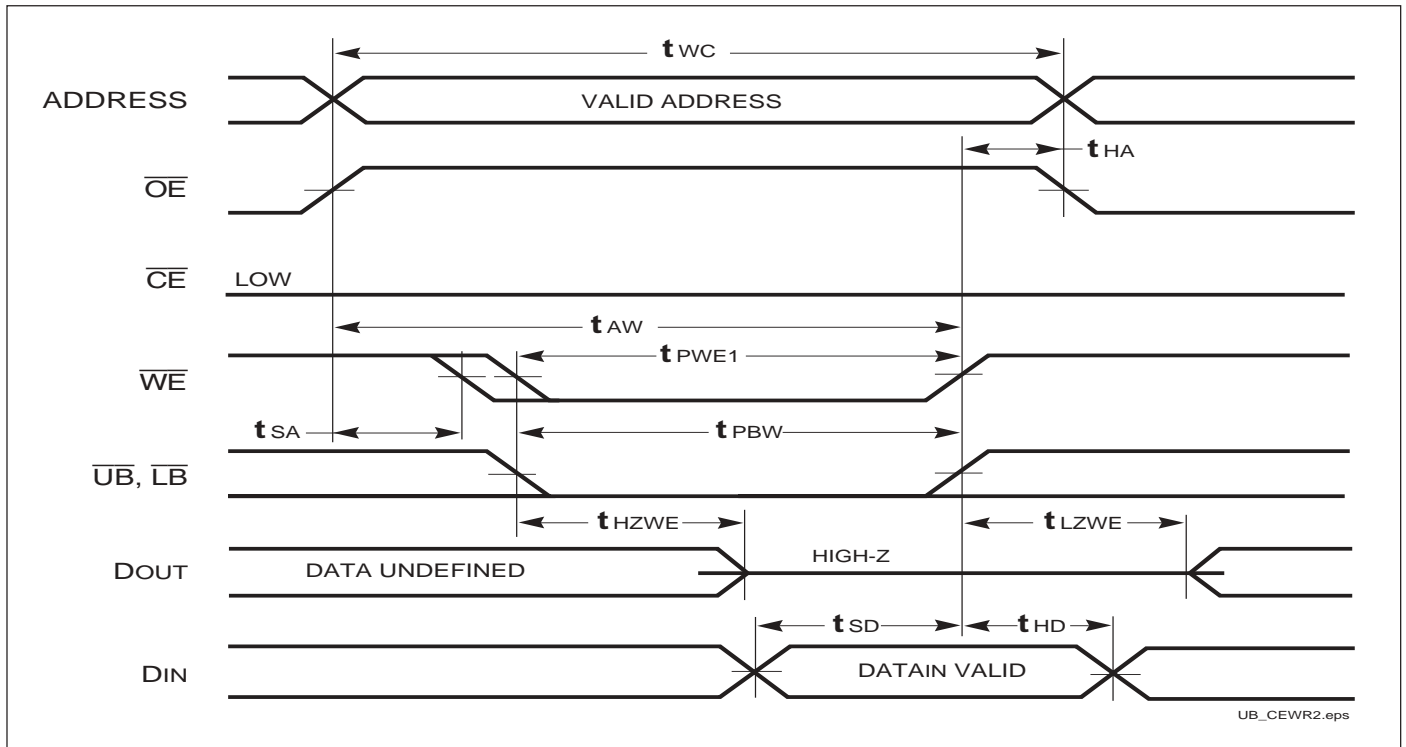
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.



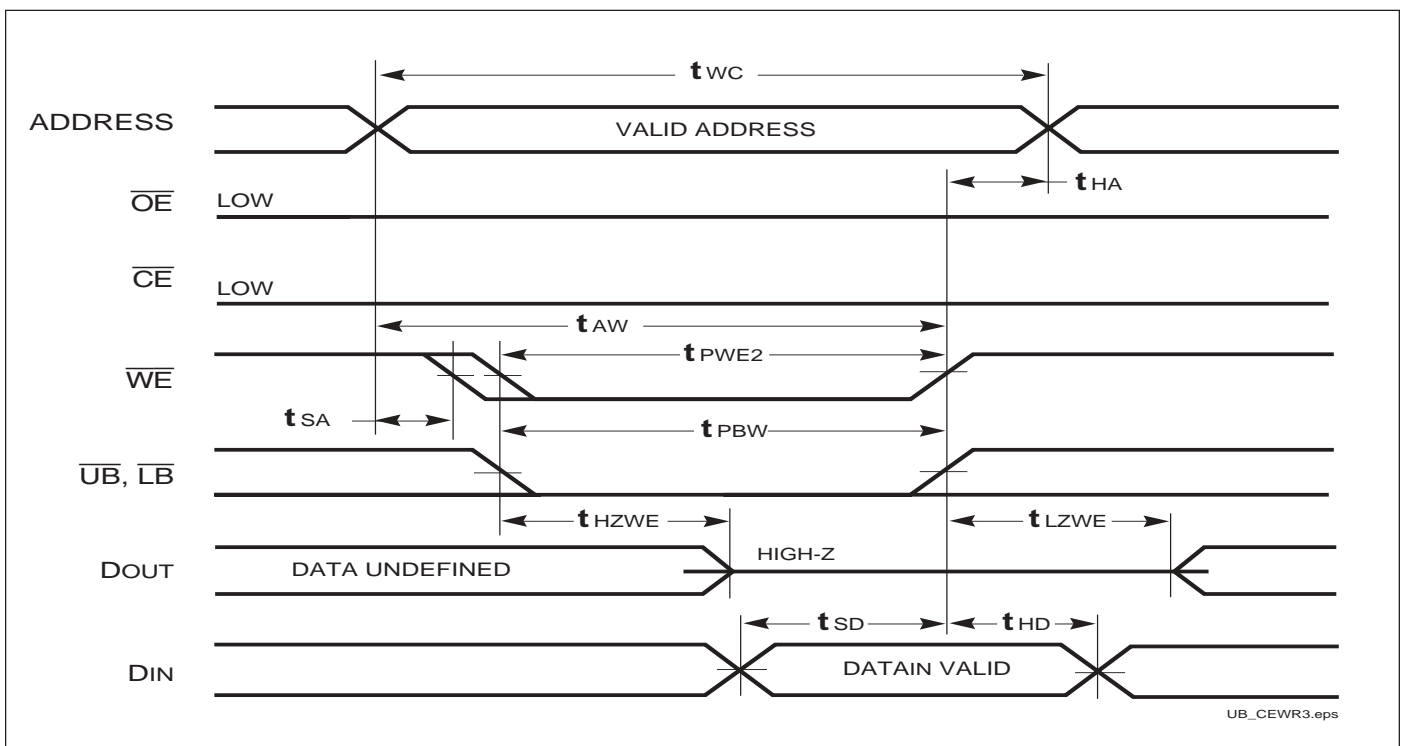
WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CE}$  Controlled,  $\overline{OE}$  = HIGH or LOW)

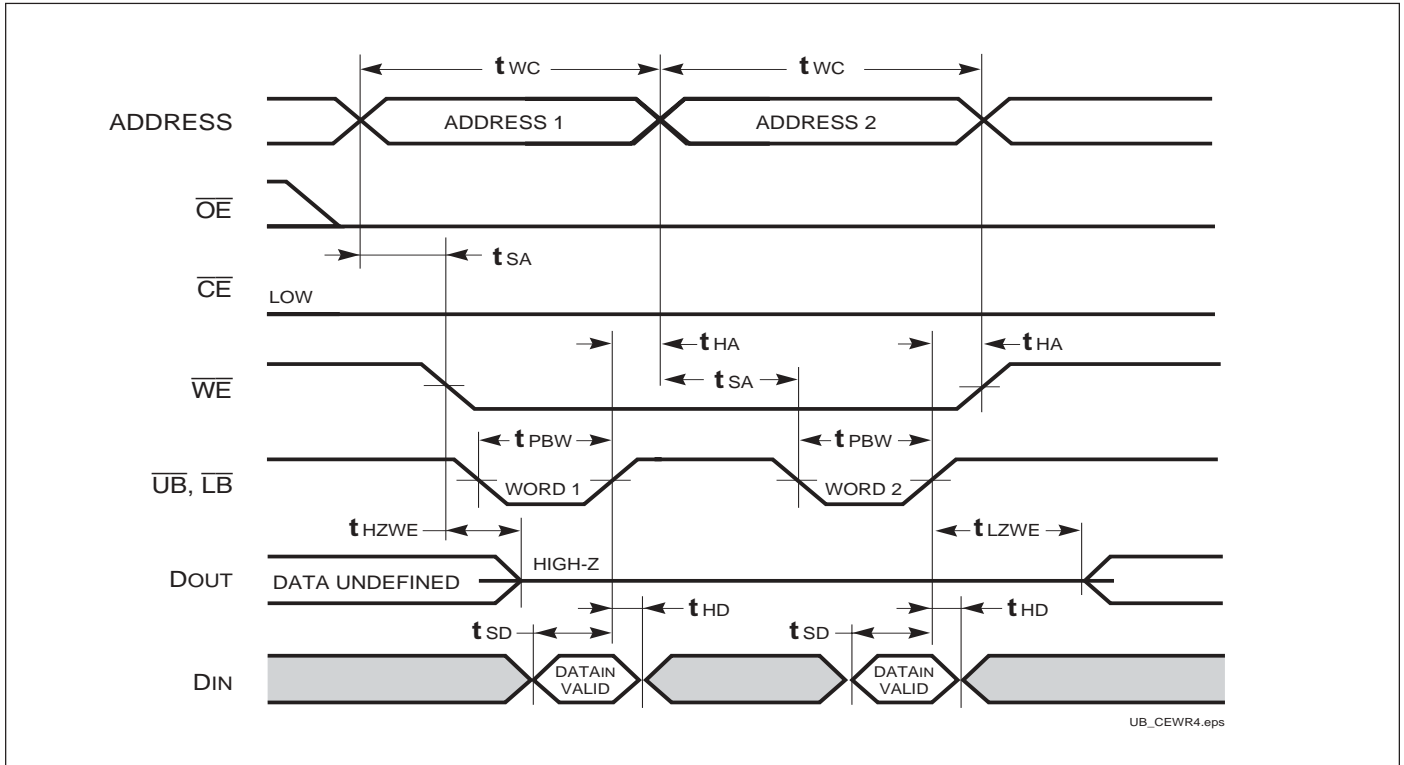


WRITE CYCLE NO. 2<sup>(1)</sup> ( $\overline{WE}$  Controlled,  $\overline{OE}$  = HIGH during Write Cycle)



WRITE CYCLE NO. 3 ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



WRITE CYCLE NO. 4 ( $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  Controlled, Back-to-Back Write) (1,3)**Notes:**

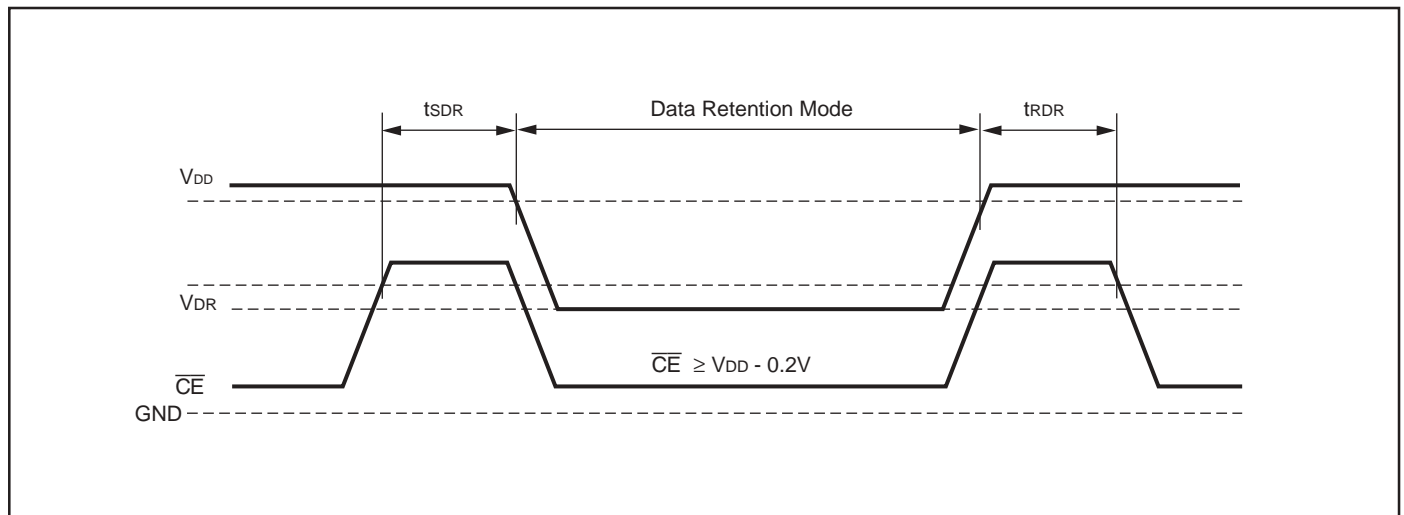
1. The internal Write time is defined by the overlap of  $\overline{\text{CE}} = \text{LOW}$ ,  $\overline{\text{UB}}$  and/or  $\overline{\text{LB}} = \text{LOW}$ , and  $\overline{\text{WE}} = \text{LOW}$ . All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The  $t_{\text{SA}}$ ,  $t_{\text{HA}}$ ,  $t_{\text{SD}}$ , and  $t_{\text{HD}}$  timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with OE HIGH for a minimum of 4 ns before  $\overline{\text{WE}} = \text{LOW}$  to place the I/O in a HIGH-Z state.
3. WE may be held LOW across many address cycles and the  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  pins can be used to control the Write function.

**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Options	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind.	— —	0.7 —	3 4	mA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform		t <sub>rc</sub>	—	—	ns

**Note 1:** Typical values are measured at V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25°C. Not 100% tested.

**DATA RETENTION WAVEFORM ( $\overline{CE}$  Controlled)**



**ORDERING INFORMATION:****Commercial Range: 0°C to +70°C**

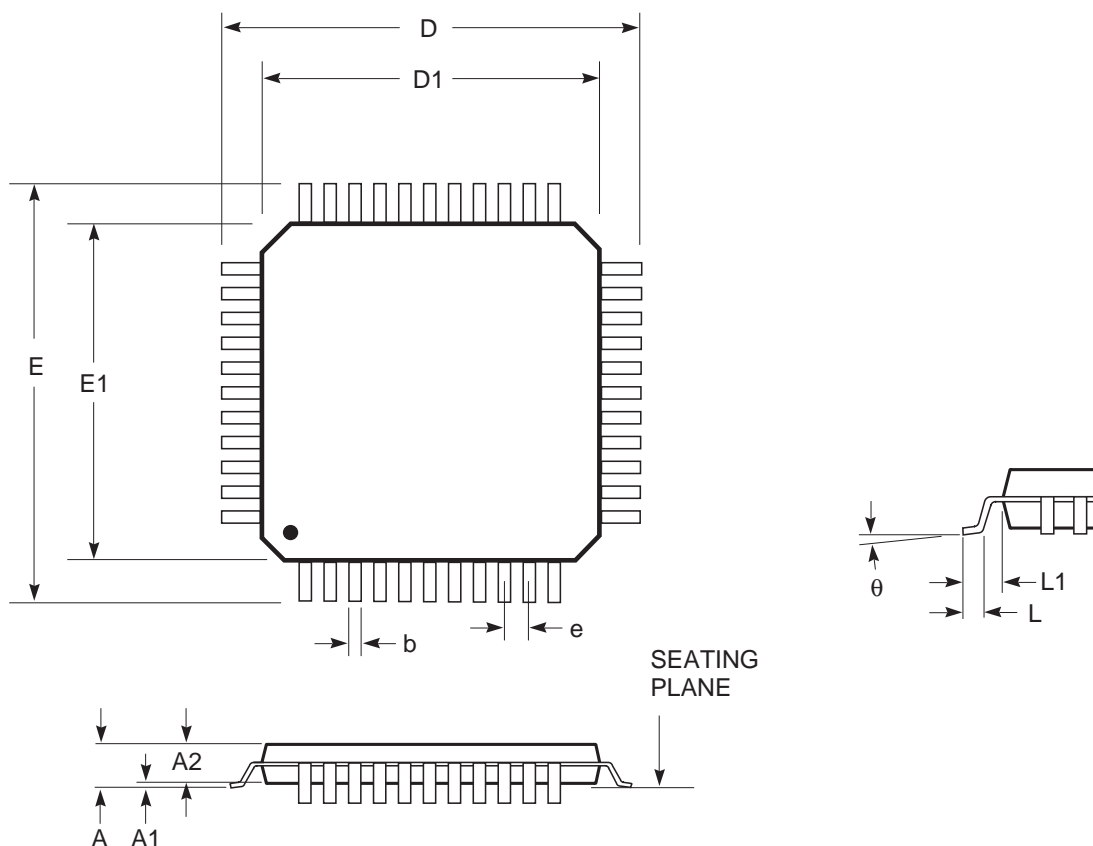
Speed (ns)	Order Part No.	Package
8	IS61LV12816L-8T	Plastic TSOP (Type II)
	IS61LV12816L-8TL	Plastic TSOP (Type II), Lead-free
10	IS61LV12816L-10T	Plastic TSOP (Type II)
	IS61LV12816L-10TL	Plastic TSOP (Type II), Lead-free

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
8	IS61LV12816L-8BI	mini BGA (6mm x 8mm)
	IS61LV12816L-8TI	Plastic TSOP (Type II)
10	IS61LV12816L-10BI	mini BGA (6mm x 8mm)
	IS61LV12816L-10BLI	mini BGA (6mm x 8mm), Lead-free
	IS61LV12816L-10LQI	LQFP
	IS61LV12816L-10LQLI	LQFP, Lead-free
	IS61LV12816L-10TI	Plastic TSOP (Type II)
	IS61LV12816L-10TLI	Plastic TSOP (Type II), Lead-free

# PACKAGING INFORMATION

**LQFP (Low Profile Quad Flat Pack)**  
**Package Code: LQ (44-pin)**



Low Profile Quad Flat Pack (LQ)				
Ref. Std.	MS-026			
No. Leads	44			
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
C	0.09	0.20	0.004	0.008
D	12.00 BSC		0.472 BSC	
D1	10.00 BSC		0.394 BSC	
E	12.00 BSC		0.472 BSC	
E1	10.00 BSC		0.394 BSC	
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.	
θ	0°	7°	0°	7°

**Notes:**

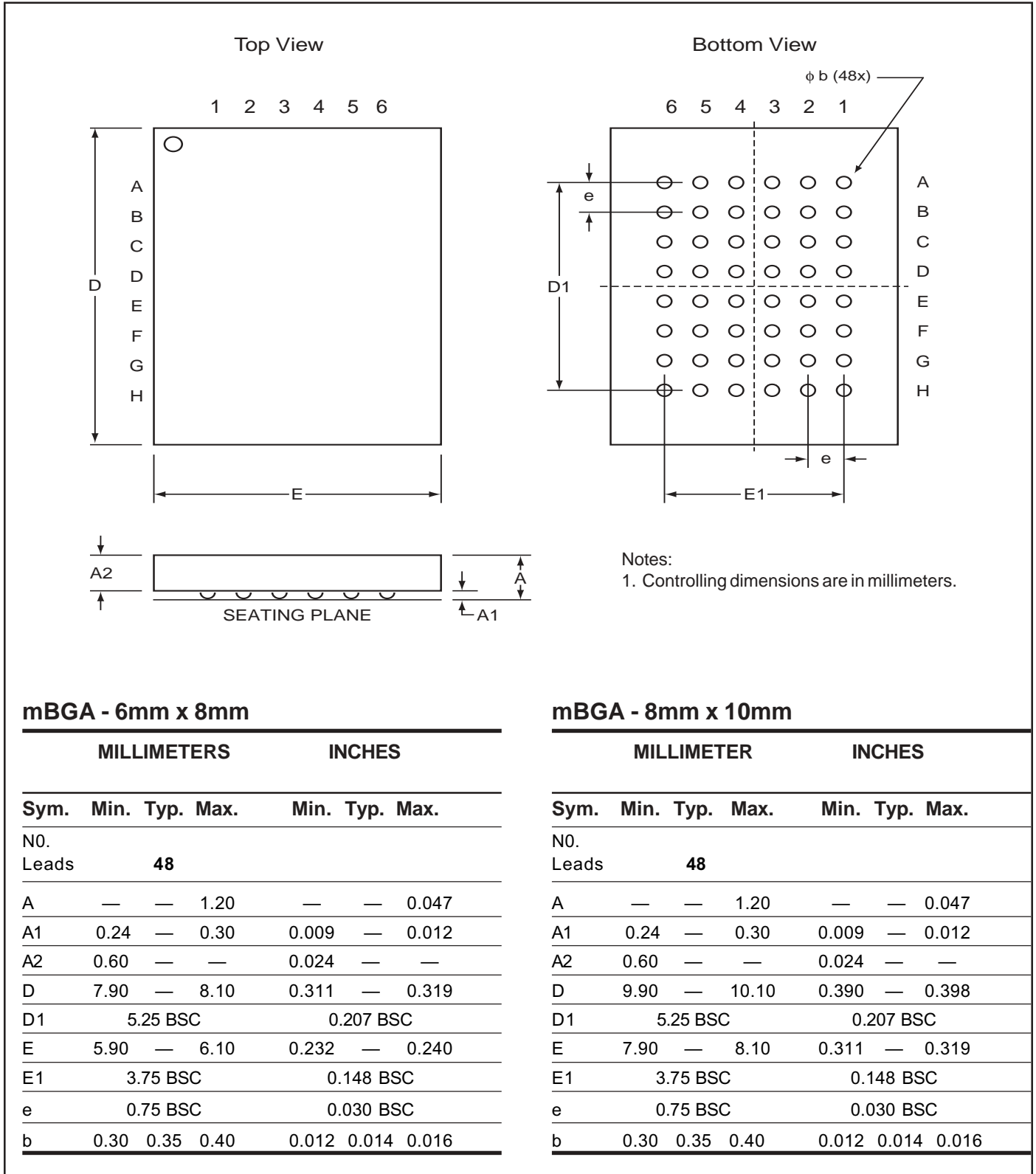
1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 include mold mismatch.
3. Controlling dimension: millimeters.

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# PACKAGING INFORMATION



## Mini Ball Grid Array Package Code: B (48-pin)



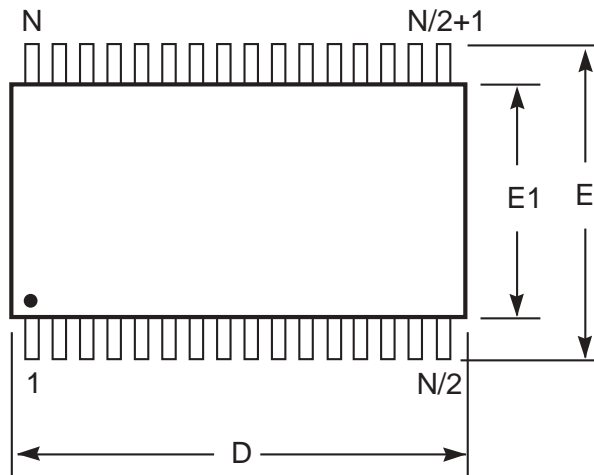
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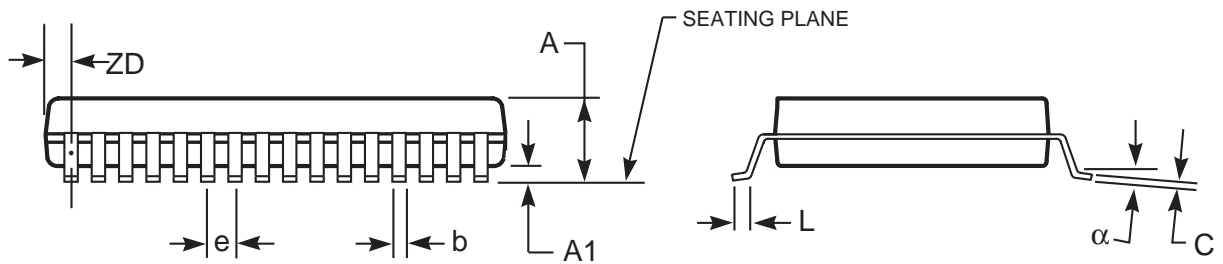
# PACKAGING INFORMATION

Plastic TSOP  
 Package Code: T (Type II)



**Notes:**

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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